FIGURE I   PRIOR ART

IC Core Logic

System Data

Mux1   Mem1   Mem2   Mux2

Serial Input

Test Data

Output Buffer
V+

Data Output

IC Output

G

Serial Output

Select 1   Control 1   Control 2   Select 2

Operation	Sample	Extest	Intest
Select 1	0100000000	0100000000	0100000000
Control 1	0CCCCCCC00	0CCCCCCC00	0CCCCCCC00
Control 2	00000000C0	00000000C0	0CCCCCCC00
Select 2	1111111111	0000000000	0000000000
		0000000000	0000000000

Figure 1A

PRIOR ART

→ TIME

IC Core Logic

System Data

Mux1   Mem1   Mem2   Test Data

Serial Input

Output Buffer
V+

Mux2

IC Output

G

Serial Output

Select 1   Control 1   Control 2   Select 2
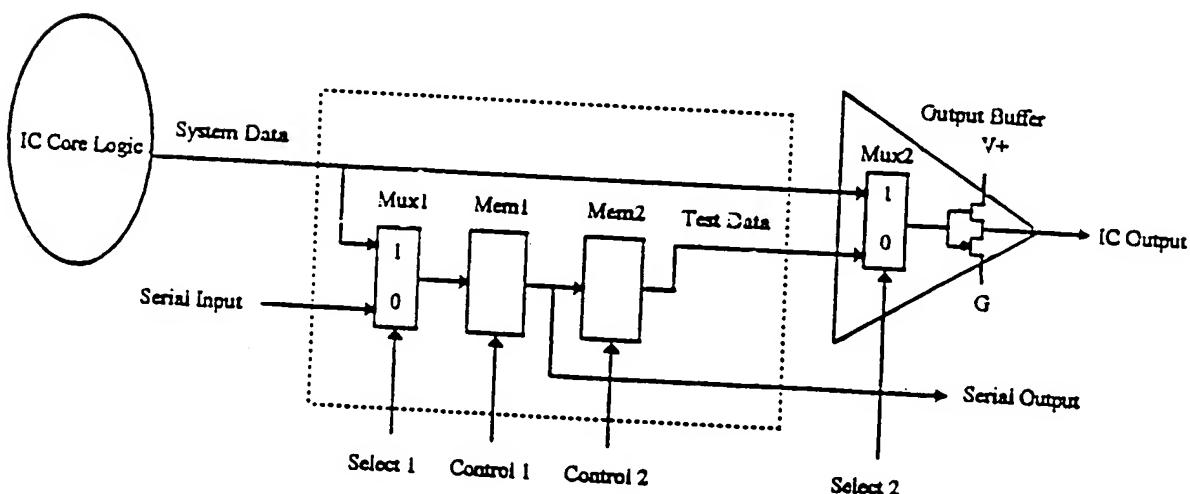
Figure 2

PRIOR ART

FIGURE 3 PRIOR ART

IC Core Logic — System Data

Mux3 Mux1 Mem1 Mem2 Mux2

Serial Input

Output Buffer V+

Data Output

IC Output

Test Data

Serial Output

Input Buffer

Select 3   Select 1   Control 1   Control 2   Select 2
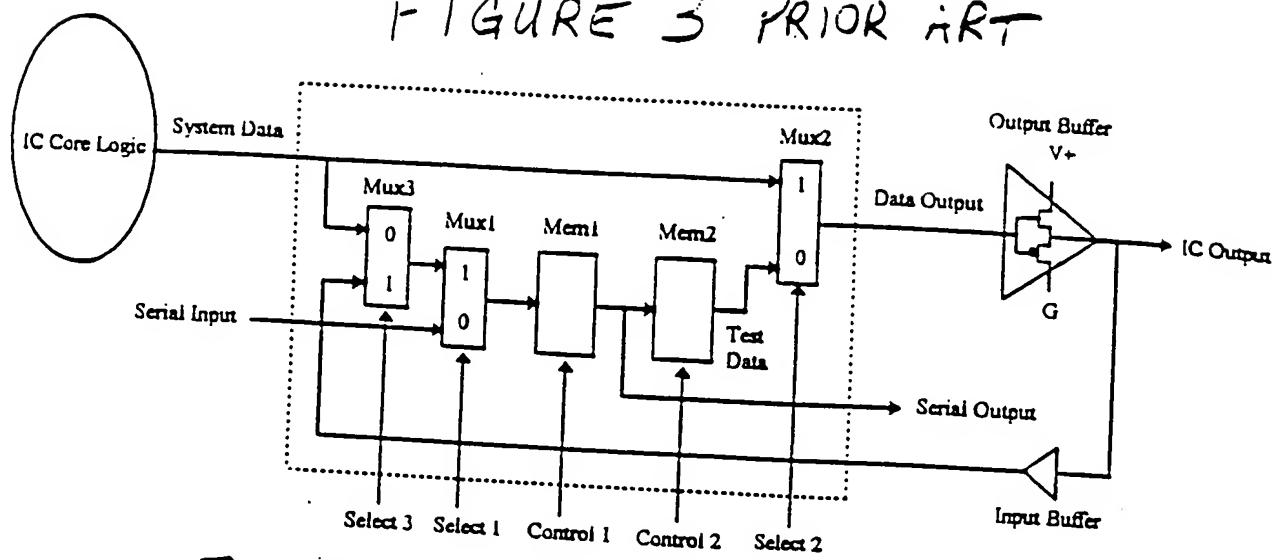
FIGURE 3A   PRIOR ART

Operation	Sample	Extest	Intest
Select 1	0100000000	0100000000	0100000000
Control 1	0CCCCCCC00	0CCCCCCC00	0CCCCCCC00
Control 2	00000000C0	00000000C0	0000000000
Select 2	1111111111	0000000000	0000000000
Select 3	0000000000	1111111111	0000000000

→ TIME

Operation	Extest1	Extest2	Extest3
Select 1	0100000000	0100	0100000000
Control 1	0CCCCCCC00	0C00	0CCCCCCC00
Control 2	00000000C0	00C0	00000000C0
Select 2	0000000000	0000	0000000000
Select 3	1111111111	1111	1111111111

Figure 3 B

→ TIME

PRIOR ART

FIGURE 4
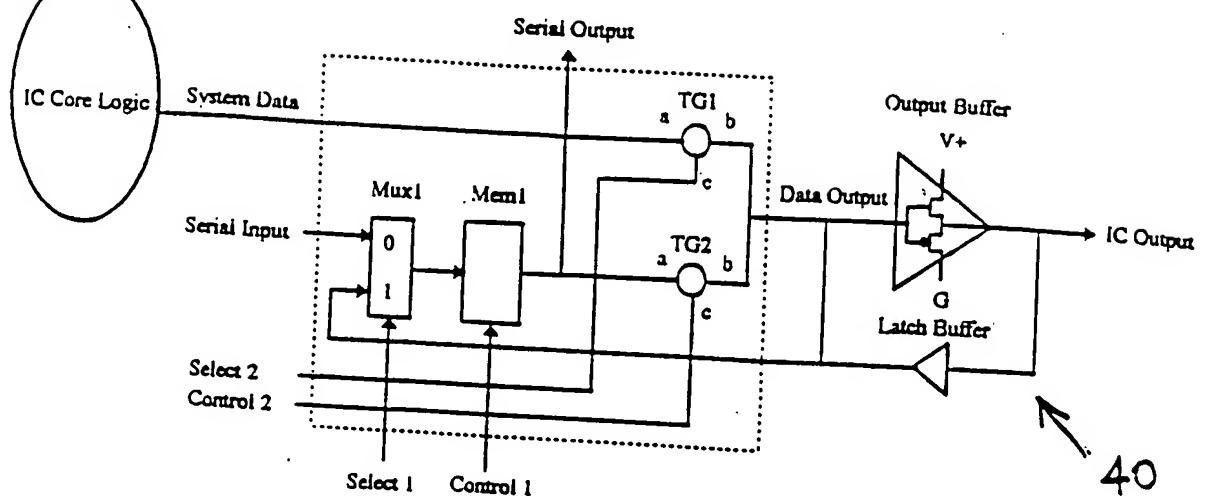
Serial Output

IC Core Logic

System Data

Serial Input

Mux1

Mem1

TG1
a   b
c

TG2
a   b
c

Data Output

Select 2

Control 2

Select 1

Control 1

Output Buffer
V+

G
Latch Buffer

IC Output

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Operation	Sample	Extest
Select 1	0100000000	0100000000
Control 1	0CCCCCCC00	0CCCCCCC00
Control 2	0000000000	00000000C0
Select 2	1111111111	0000000000

FIGURE 4A →TIME

Operation	Extest
Select 1	0100000000
Control 1	0CCCCCCC00
Control 2	1000000011
Select 2	0000000000

Figure 4B → TIME

Transmission Gate used for TG1 & TG2

a   b
c
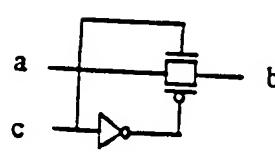
Tristatable Buffer used for TG1 & TG2

a   b
c

Figure 5

FIGURE 6

40
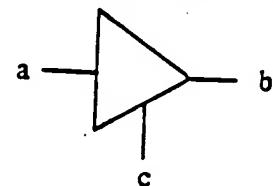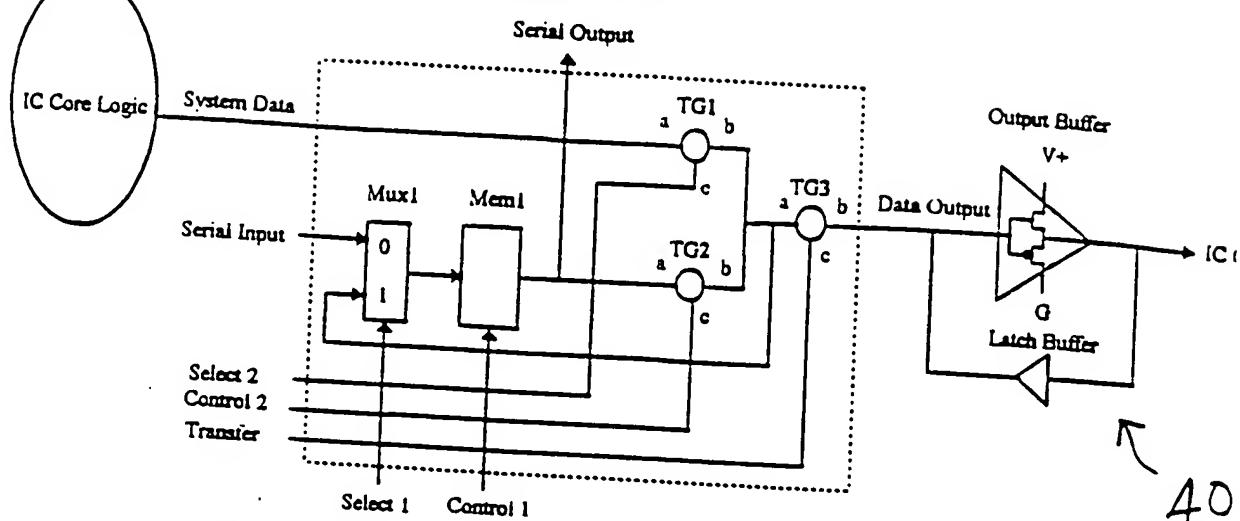
FIGURE 6A

Operation	Sample	Extest	Intest
Select 1	0100000000	0100000000	0100000000
Control 1	0CCCCCCC00	0CCCCCCC00	0100000000
Control 2	0000000000	00000000C0	0CCCCCCC00
Select 2	1111111111	0000000000	00000000C0
Transfer	1111111111	01000000C0	0100000000
			00000000C0

→ TIME

| Operation	Extest	Intest
Select 1	0100000000	0100000000
Control 1	0CCCCCCC00	0CCCCCCC00
Control 2	1000000011	1000000011
Select 2	0000000000	0100000000
Transfer	1100000011	1000000011

Figure 6 B → TIME
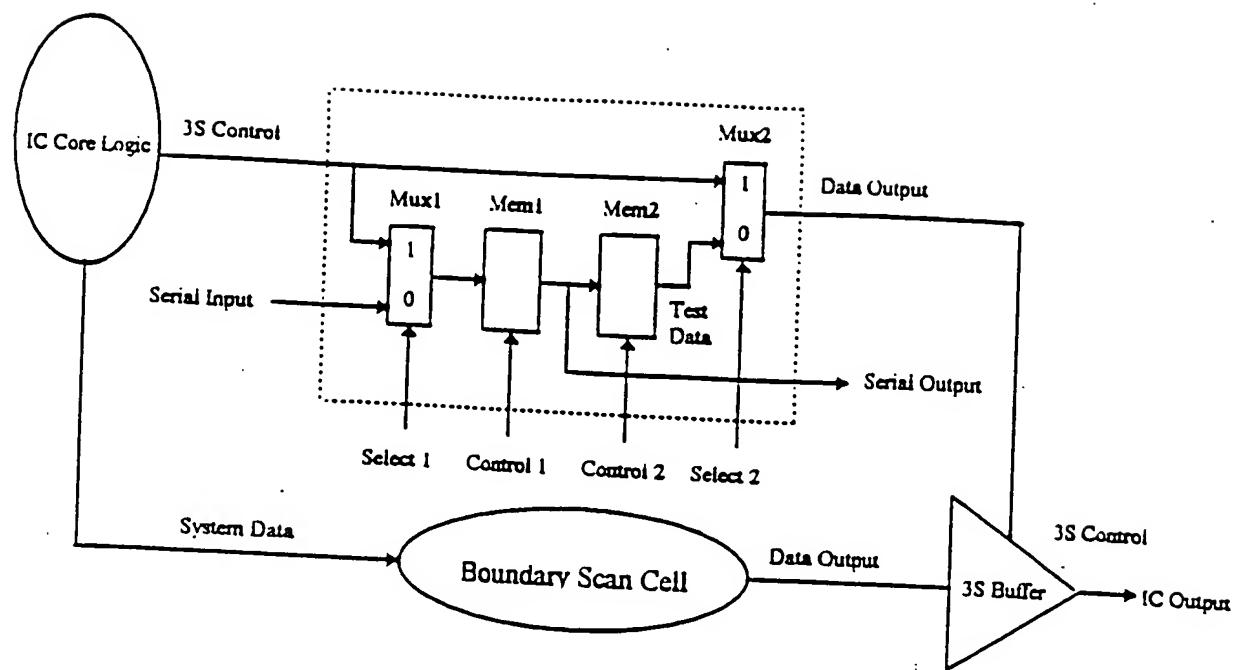
Figure 7

PRIOR ART

Figure 8

Input Buffer

V+

IC Input

System Data

Mux1   Mem1   Mem2   Mux2   Data Buffer   Data Input   IC Core Logic

1

G

0

Serial Input

1

0

Test Data

Serial Output

Select 1   Control 1   Control 2   Select 2

Figure 9   PRIOR ART

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103

101

TG1

Input Buffer

V+

IC Input

a   b

c

Data Input   IC Core Logic

G

Latch Buffer

Select 2

100

Mux1   Mem1

1

0

TG2

a   b

c

Serial Input

Control 2

Serial Output

Select 1   Control 1

Figure 10

103

111
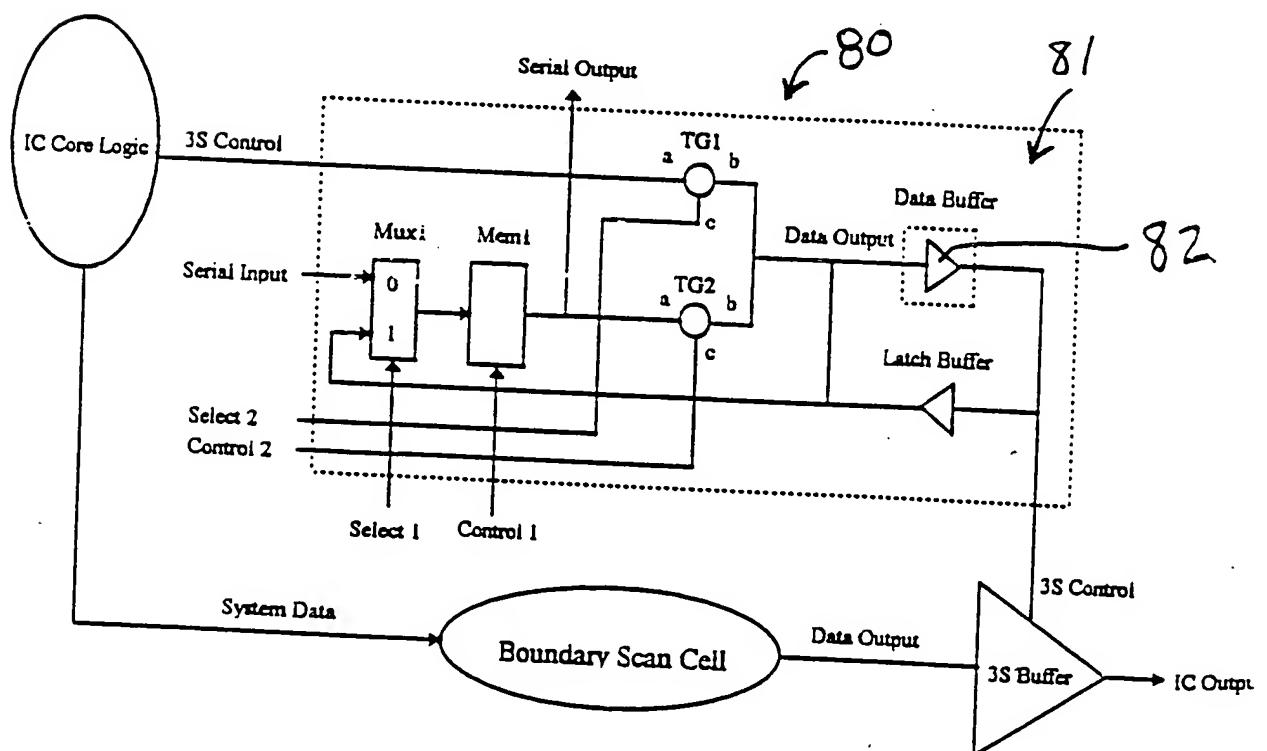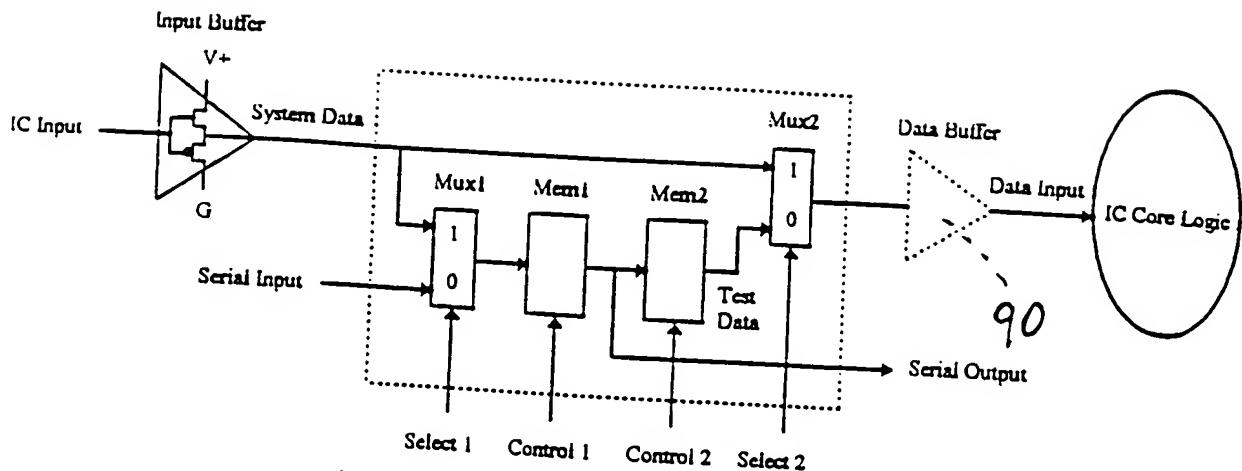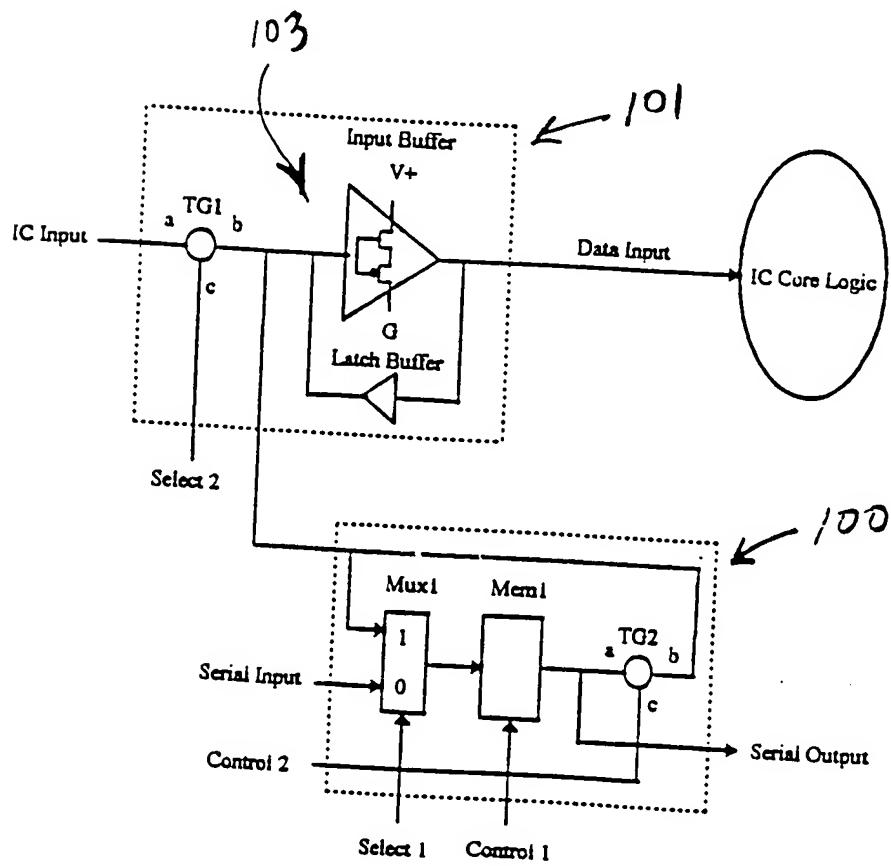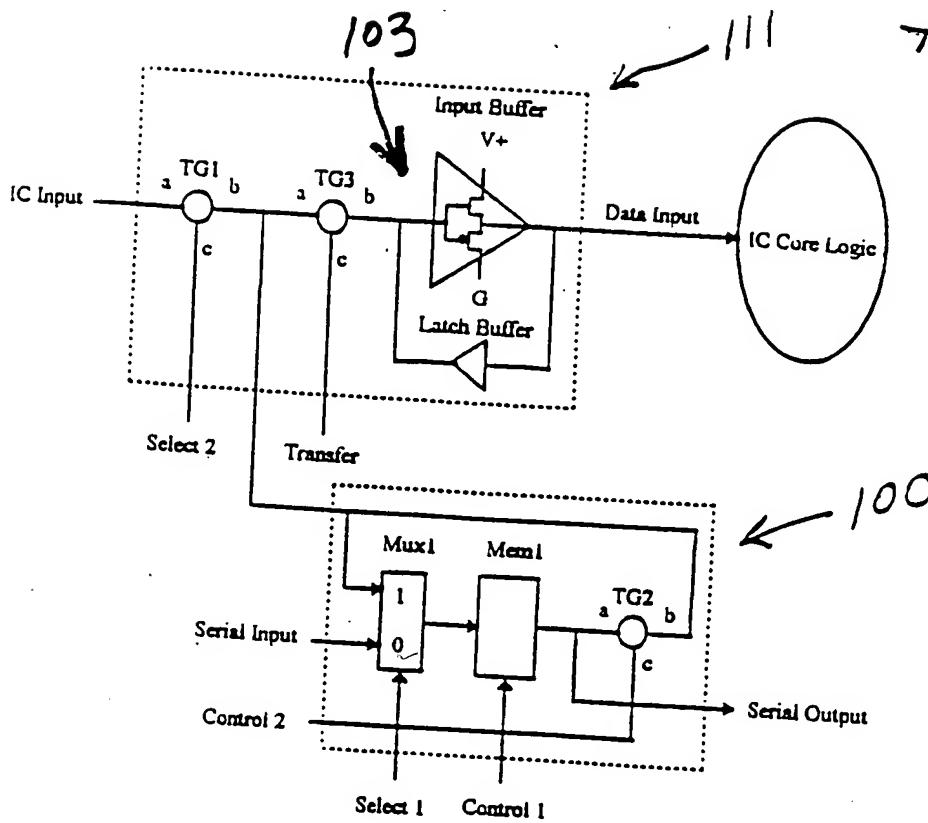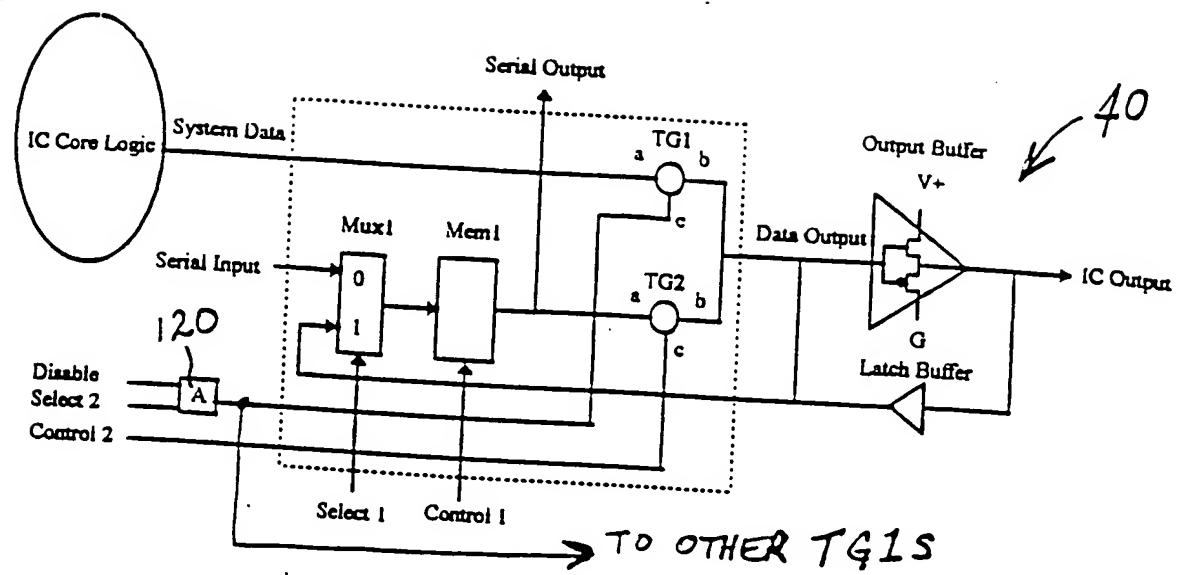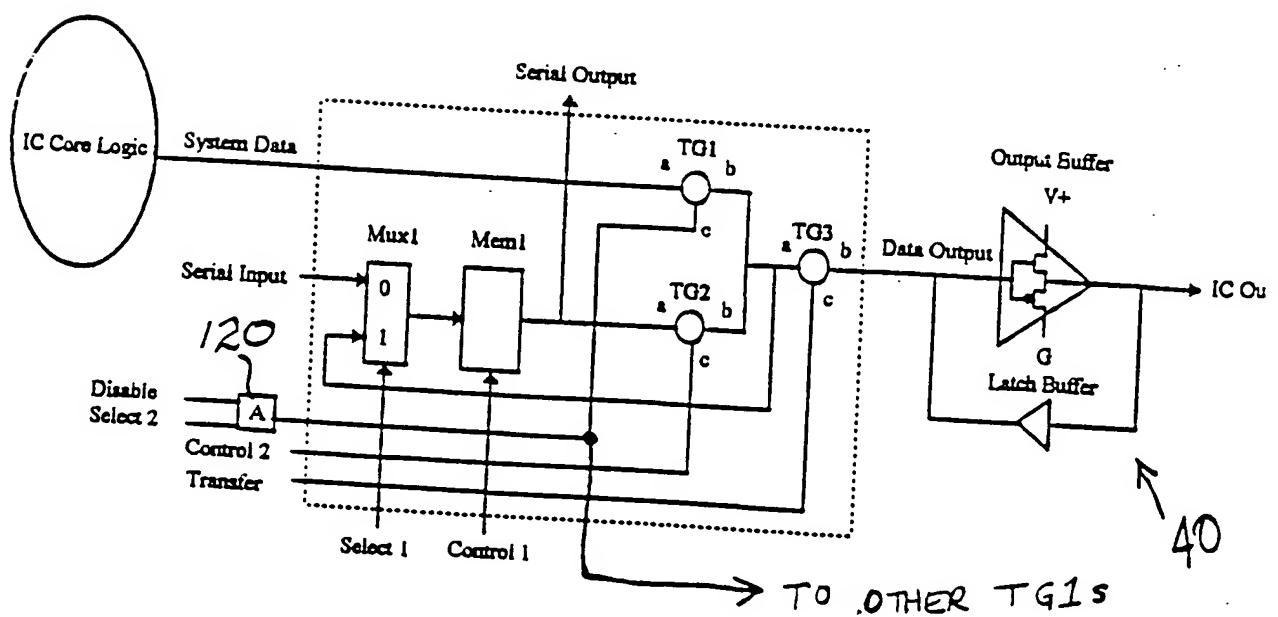
Figure 11

FIGURE 12

Figure 13

Figure 14

Figure 15

Figure 16